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SECOND QUARTERLY PROGRESS REPORT
FOR
UHF DUPLEXERS
SEMICONDUCTOR EFFORT

5 February 1963 - 5 May 1963

Contract NObsr 89105
Project Serial No. SF 0010205
Task No. 6158

Department of the Navy
Bureau of Ships
Electronics Divisions

MICROWAVE
ASSOCIATES,
INC.

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MICROWAVE ASSOCIATES, INC.
Burlington, Massachusetts

NAVY DEPARTMENT BUREAU OF SHIPS ELECTRONICS DIVISIONS

CONTRACT NObsr 89105
PROJECT SERIAL NO. SF 0010205
TASK NO. 6158
July 10, 1963

Prepared by:

Joseph White
Microwave Circuit Engineer
Solid State Division

Sumner Segal
Ferrite Project Engineer
Solid State Division

Approved by:

M. E. Hines
Division Manager
Solid State Circuit Division

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ABSTRACT

The design criteria for an optimum semiconductor receiver protector circuit are presented. Using these criteria the characteristics of a self-switching PIN diode limiter for use in the 420 Mc range are derived. Measured data on a four diode switch are presented and compared with the program requirements.

Two approaches to the 420 Mc circulator design are described along with measurements of high power and low power performance.

PART I

PURPOSE

The purpose of this program is to develop high power duplexers at 210 and 420 Mc. The complete duplexer will consist of a ferrite circulator followed by a semiconductor limiter chain. Designs for pulse powers up to 1 Mw, CW powers to 10 KW, and pulse widths up to 200 μsec are being followed.

DETAILED FACTUAL DATA

A. Ferrite Circulator Tests

During the second quarter of this development program, several tests were conducted in an effort to complete the design of a three port circulartor at 420 mc/s capable of handling 300 kw peak, 3000 watts average, power.

The basic approach consisted of two different mechanical design features, both of which utilized the same type of garnet material. The first configuration shown in Fig. 1a consisted of two thick discs of Trans Tech G1002 gadolinium doped garnet material and the other utilized tapered ground planes with thinner discs of garnet. When using the .400" thick disc, it was realized that the advantage gained by its ability to handle higher peak power could be offset by the units ability to dissipate the heat within the garnet.

The unit shown in Fig. 1a was constructed and tests performed at low power to optimize performance by matching techniques and dc bias above resonance. Using two discs of G1002, 2.420" diameter by .400" thick, and various junction matching configurations the circulator produced the results shown in Fig. 2. There is no question that better performance could have been attained by improvements in the junction impedance, but at this stage of the development, it was considered advisable to run some high power measurements to determine whether or not this approach was realistic. Therefore, the circulator was run at 500 watts CW and data recorded at various time intervals. The performance curves are shown in Fig. 3 and indicate that the predicted

temperature stability of G1002 has been obtained.

While the unit shown in Fig. 1a was being high power tested, the unit of Fig. 1b was fabricated. The lower level tests, conducted to optimize performance at 425 mc/s, produced results that were most encouraging. With half the thickness of garnet material being used, it is anticipated that the rate of heat transfer would be increased by a factor of two. Several high power tests were conducted up to a maximum of 1500 watts CW with no radical change in performance. (See Fig. 4) However, in order to transmit the equivalent of 3000 watts of average power, it may be possible that water cooling will be required.

Several designs have been considered for improvement of heat removal. Fig. 1a shows one possibility for an air cooled unit. Such a design would increase the overall weight and height by a small amount due to the increase in magnet gap, but in turn will provide for excellent heat transfer. The alternative to the air cooled design is shown in Fig. 1b. Here, a one-quarter inch square tube was brazed on top of the ground places and around the magnets. The amount of heat removed will be a function of the water temperature and flow rate and its effectiveness will be measured at a later date.

Pulsed power tests have not been conducted on the above circulators at this time. First of all, in order to conduct this type of test, modifications must be made to the center conductor. The copper matching sheets must be removed and replaced by its equivalence in form of a center conductor of solid brass or copper with a similar junction configuration. Secondly, since the average power problem is considered

more difficult to overcome, the final design of the circulator will depend on how this problem is solved. The 300 kw peak power requirement for this particular phase of the program does not present any foreseeable difficulties.

During the next quarter, a 420 mc/s circulator capable of performing over a 10% bandwidth with isolation, insertion loss and VSWR all within the specifications set forth by the Microwave Associates proposal will be completed. The preliminary design of the 200 mc/s circulator should progress to a point where parts may be purchased. The design of the lower frequency unit will depend on test data gathered at the 420 mc/s circulator when CW power of 5 kw and peak power of 1 MW are transmitted through the device.

B. Semiconductor Circuit Design

In the last quarterly progress report data was cited which typified the self-limiting behavior of an opposed polarity diode pair mounted in shunt with a 50 ohm transmission line. It was seen that an incident peak power, at about 420 megacycles, of 8 kilowatts with a pulse length of 5.5 microseconds and a duty cycle of 0.001 was withstood. The isolation, or limiting, reached a value of 21 db, although an isolation value of 33 db was obtained when the diodes were pre-biased with an externally applied dc current. In this quarter investigations were made to ascertain the optimum circuit that may be designed to exploit fully the capability of the diodes used. For this design it was assumed that diodes used would be externally biased since this assures the maximum diode impedance switching ratio. It is believed that the circuit so

developed will yield a good form from which to evaluate self biased performance also.

Investigations to study the limiting behavior of thin I region PIN diodes will be carried on concurrently so that the feature of a self-biased receiver protector may be incorporated in the final engineering models. However, at this time it is believed that optimum performance in terms of isolation and insertion loss, as well as power handling capacity, will be achieved -- for any particular circuit and diode -- when an externally applied bias is used.

In the following discussion presentation is made of the design criteria for an optimum semiconductor receiver protector circuit. Measured results for a four diode switched receiver protector are cited and details of a circuit to exploit these results is presented.

1. Theoretical Consideration of the Ideal Duplexer*

a) Functional Constraints: The requirement of a duplexer is the same as that of a SPST switch in that it is a two-port required to transmit incident energy with minimum insertion loss in one state and to reflect it principally in the other. However, the transmission state need sustain only "signal level" power. A further distinction exists in that the duplexer is often required to be self-switched to the isolation state by the incident high power; but for this discussion it will be assumed the switch element, here chosen to be a diode, reaches its transmission and isolation states in some way or other; and the

*Part of this analysis was performed under Contract AF 30(602)-2656, "Application of Semiconductor Devices to High Power Duplexers"

resultant RF capability will be evaluated.

It is assumed that the duplexer has two constraints, namely, that there is a maximum power, P_d, which may be dissipated in the forward biased diode switch element and that there is a maximum insertion loss, $I.L._m$, which is permitted in the transmission state of the diode -- the diode may be zero or reverse biased for this state. The turns ratio, n_3, of the transformer shown in the duplexer circuit of Fig. 5 is chosen so that for the switch element shown P_d and $I.L._m$ are achieved in the isolation and transmission states respectively. The method for choosing n_3 and the maximum incident line power, P_L, will now be determined.

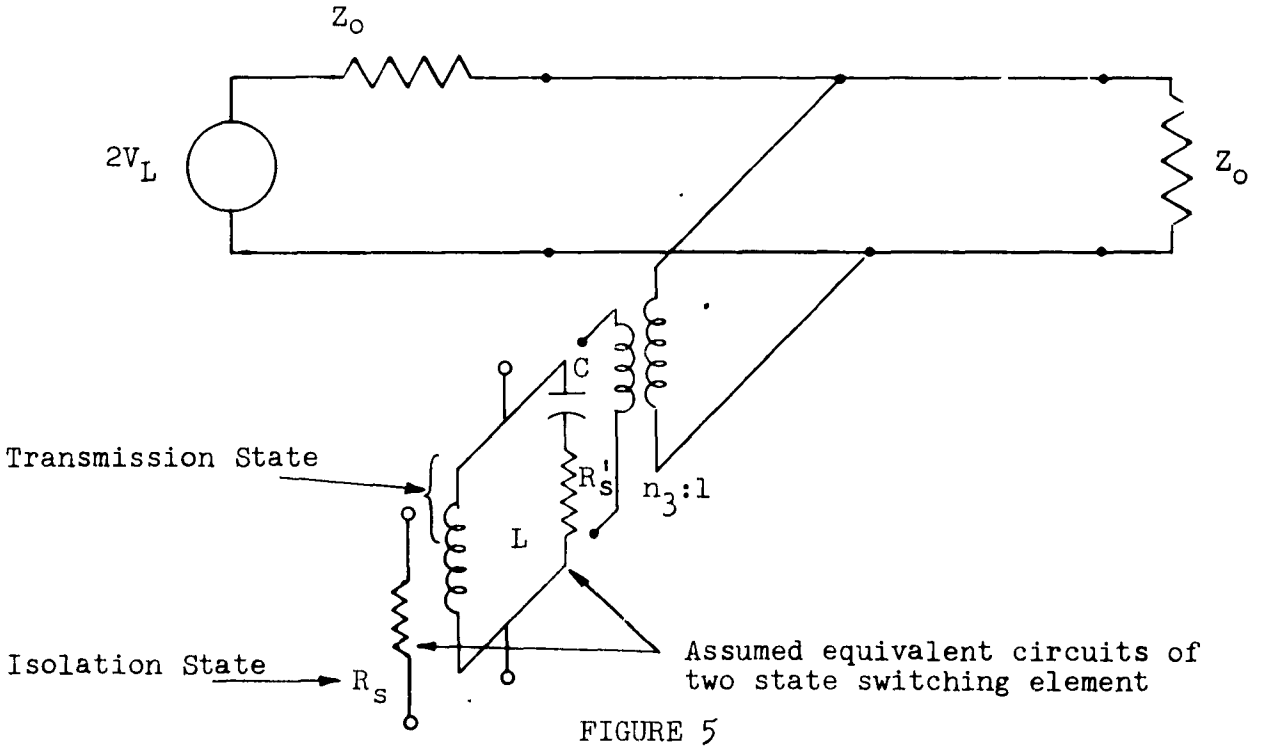


FIGURE 5

b) Exact Solution: The method for determining n_3 is to relate it to the allowable insertion loss, $I.L._m$. Then the duplexer circuit

is completely defined and the maximum power sustainable is readily determined.

Refer to Figure 5, and consider the transmission state.

$$\text{Let } Q = \frac{1}{\omega C R_s'} \tag{1}$$

Select L to parallel resonate the capacitive susceptance.

$$\text{i.e. let } \left|\frac{1}{\omega L}\right| = \left|\frac{Q}{R_s' (1 + Q^2)}\right| \tag{2}$$

Then a normalized conductance, $\bar{g}$, appears across the main transmission line, and the resulting insertion loss is given by

$$(\text{I.L.}) = \left|1 + \frac{\bar{g}}{2}\right|^2 \tag{3}$$

$$\text{where} \qquad \bar{g} = \frac{1}{R_s' (1 + Q^2)} \times n_3^2 \times Z_o. \tag{4}$$

Once n_3 has been chosen to cause

$$\text{I.L.} = \text{I.L.}_m \tag{5}$$

then the power dissipated in the diode, P_d, can be determined as a function of the incident power (when the diode is in the reflecting,

or isolating, admittance state). This is easily determined using the equivalent circuit of Fig. 6.

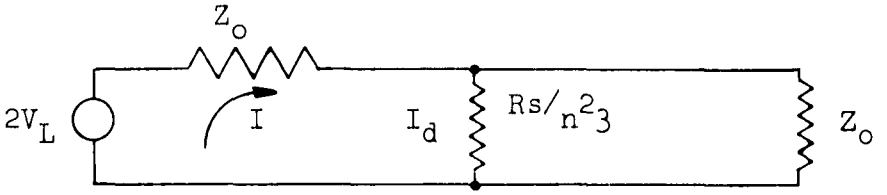


FIGURE 6

$$I = \frac{2V_L}{Z_o}\left(\frac{1}{1+\frac{1}{1+Z_o n_3^2/R_s}}\right) \tag{6}$$

$$I_d = I\left(\frac{n_3^2/R_s}{n_3^2/R_s + 1/Z_o}\right) \tag{7}$$

$$P_d = I_d^2 \frac{R_s}{n_3^2} \tag{8}$$

$$P_L = V_L^2/Z_o \tag{9}$$

Having chosen n_3 to satisfy Equations (3), (4) and (5) and having determined the maximum incident power, P_L, the isolation that is obtainable in the reflecting state is found as follows.

$$\text{Isolation} = \overline{\text{I.L.}} = \left| 1 + \frac{\bar{g}}{2} \right|^2 \tag{10}$$

$$\bar{g} = \frac{Z_o n_3^2}{R_s} + 1 \tag{11}$$

c) Approximate Solution: The values P_d and I.L._m calculated previously can be determined approximately, as will be shown, resulting in further insight into the duplexer limits. It should also be pointed out that both the exact and approximate calculations made to determine duplexer insertion loss and isolation are equally valid for the case of a SPST Switch representable by the equivalent circuit of Figure 5.

(i) Insertion Loss in Transmission State

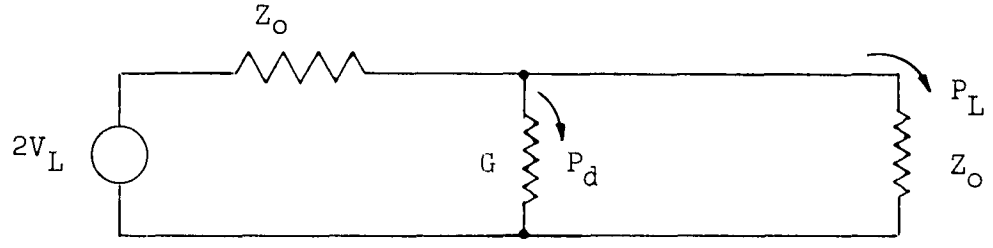


FIGURE 7

$$G = \frac{n_3^2}{R_s' (1 + Q^2)} \approx \frac{n_3^2}{R_s' Q^2} \tag{12}$$

Assume $G << 1/Z_o$

Then

$$I.L. \approx \frac{V_L^2 G}{I_L^2 Z_o} \approx \frac{V_L^2 n_3^2}{I_L^2 Z_o R_s' Q^2} = \frac{P_L Z_o n_3^2}{P_L R_s' Q^2} = \frac{Z_o n_3^2}{R_s' Q^2} \tag{13}$$

Select n_3 so that $I.L. = I.L._m$

Then

$$n_3^2 \approx \frac{(I.L._m)\, R_s' Q^2}{Z_o} \tag{14}$$

(ii) Power Dissipated in Isolation State

The line power, P_L, is given by:

$$P_L = V_L I_L = V_L^2 / Z_o \tag{15}$$

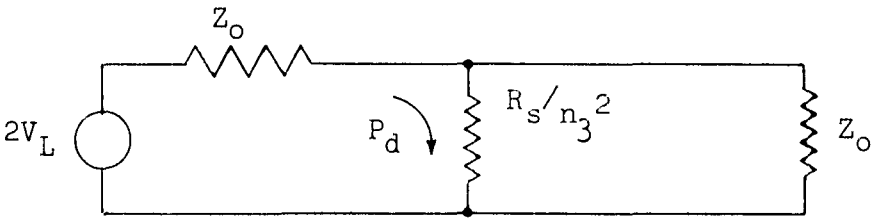


FIGURE 8

Assume $\frac{R_s}{n_3^2} << Z_o$

Then

$$P_d \approx (2I_L)^2 \frac{R_s}{n_3^2} \tag{16}$$

$$P_d/P_L \approx \frac{4R_s}{Z_o n_3^2} \tag{17}$$

(iii) Maximum Switchable Power: Substitute result for n_3^2 obtained in Equation (14) into Equation (17).

$$P_d/P_L = \frac{4R_s}{Z_o} \cdot \frac{Z_o}{(I.L._m)\ R_s' Q^2} \tag{18}$$

$$P_L \approx \frac{P_d\ (I.L._m)\ Q^2 R_s'}{4R_s} \tag{19}$$

Equation (19) defines the maximum allowable incident power, P_L, which may be sustained by the duplexer in terms of the diode limitations only -- the approximations made to obtain it did not circumvent any non-ideal circuit behavior. The result is actually more general, in that Equation (19) is true even if the values P_L, (I.L.) and P_d were not maximized.

Therefore, the duplexer circuit described is optimum. It is not unique, and other optimum circuits may be found which would yield as good but not better results.

(iv) Approximate Values of Isolation and Insertion Loss: The approximate insertion loss and isolation are seen from the equivalent circuits shown in Figures 7 and 8 respectively.

$$\text{I.L.} - \left|1 + \frac{\bar{y}}{2}\right|^2 \tag{20}$$

$$\bar{y} = \bar{g} = \frac{n_3^2 Z_o}{R_s' (1 + Q^2)} \tag{21}$$

Assume $Q^2 >> 1$

Assume $\bar{g} << 1$

$$\text{Insertion Loss} \approx 1 + \bar{g} \tag{22}$$

$$\text{Insertion Loss} \approx 1 + \frac{n_3^2 Z_o}{R_s' Q^2} \tag{23}$$

To determine the isolation,

$$\bar{g} = \frac{Z_o n_3^2}{R_s} \tag{24}$$

$$\text{Assume } \frac{Z_o n_3^2}{R_s} >> 1$$

then

$$\text{Isolation} = \overline{\text{I.L.}} \approx \frac{\bar{g}^2}{4} \tag{25}$$

$$I.L. \approx \frac{1}{4}\left(\frac{Z_o n_3^2}{R_s}\right)^2 \qquad (26)$$

2. Diode Characterization: An evaluation of the PIN diode type believed most suitable for use as a self-limiting receiver protector in the UHF frequency range was made. Pertinent data is included below in Table I.

TABLE I

Diode Description:

Type	PIN
I Region Thick	0.5 mil. approx.
Junction Dia.	30 mil. approx.
Die Height	2 mil. approx.

RF Parameters:

R_S, Resistance	@ +100 ma	bias,	0.32 ohms
R_S, Resistance	@ 0	bias,	12.5 ohms
C, Capacitance	@ 0	bias,	5 pf approx.
Q,	@ 0	bias,	6 pf

As can be seen, the parameters discussed in Section II were evaluated and from them, together with a measure of the dissipating capability of the diode, a duplexer circuit can be designed.

At the same time measurements were made of a receiver protector consisting of a single pole single throw switch which simulates one arm of a balanced semiconductor limiter chain. Pertinent details of this test are seen in Table II.

TABLE II

Diode Parameters

Type	Pin
Number Used	4
I Region Thcikness	4 mils approx.
Junction Diameter	30 mils approx.
Breakdown Voltage	1000 volts
Resistance @ +100 ma bias	0.5 ohms
Capacitance @ 0 bias	2.5 pf @ IMC

RF Performance

Switch Configuration	4 Diodes Shunting Line at same plane
Line Impedance	50 ohms
Frequency	420 MC
Peak Power Incident	60 kilowatts
Average Power Incident	60 watts
Pulse Length	6 microseconds
Isolation @ +100 ma bias/diode	40 db
Insertion Loss (zero bias)	1.4 db
Insertion Loss (-100v bias)	0.4 db

These results are to be compared with the desired objectives for the semiconductor single limiter chain listed below in Table III.

TABLE III

Requirements of 420 MC Single Limiter Chain

Frequency	420 MC
Bandwidth	10 %
Isolation (to assure receiver power less than 100 mw peak)	55 db
Insertion Loss	0.5 db max.
Peak Power	15 kilowatts
Average Power	150 watts
Pulse Length	60 microseconds

Comparison of Tables II and III shows that achieved results, although exceeding the required performance in peak power, lack the average power and pulse length required capabilities. Furthermore, a larger switching ratio is required, that is, higher isolation and reduced insertion loss at zero bias. The switch circuit described by Table II was tested to 60 kilowatts peak power without failure of any of its four diodes. Testing of a switch model at 60 microsecond pulse lengths will be performed in the coming quarter since this facility is now nearing completion at Microwave Associates.

The detailed calculations and design criteria of a receiver protector to accomplish the desired performance at 420 megacycles utilizing the information discussed in Section 1 follows.

3. Detailed Design Criteria of Semiconductor Receiver Protector

It was shown in Section 1 that once the allowable receiver protector insertion loss and diode power dissipating capability can be determined, then the maximum line power which a circuit of proper design can sustain is given by Equation (19) which is repeated below

$$P_L = \frac{P_d (I.L._m)\ Q^2 R_s'}{4\ R_s} \qquad (19)$$

The following will present a solution to this equation based on the desired parameters of this system.

First, it is necessary to evaluate P_d, the maximum power which may be dissipated by a single diode. To do this consider Table IV which summarizes the geometric and thermal properties of a single semiconductor die.

TABLE IV

Diameter of Semiconductor die	0.030 inches
Height	0.002 inches
Volume	1.4×10^{-6} cu inches
	2.4×10^{-5} cm^3
Density (Silicon)	2.4 gm/cm^3
Specific Heat (Silicon)	0.21 cal/gm x ^{o}C

If, then, it is assumed that no cooling takes place during the period of an RF pulse then some maximum energy value may be calculated which will just cause the temperature of the semiconductor die to be elevated above the ambient by 200^{o} centigrade, which is here assumed to be the maximum non-destructive operating temperature level. This may be found from the previous table to be 0.01 watt seconds, and this is the amount of energy which may be dissipated in the semiconductor die in a single RF pulse. Since a pulse length of 60 microseconds is desired, the maximum power dissipation in the diode is limited to 160 watts. This together with the previous diode characterization data included in Table I, may be used to calculate the maximum duplexer power sustainable per diode. Rewriting these results as seen in Table V.

TABLE V

P_d/diode =	160 watts
I.L. (max.) =	0.5 db = 0.1
Q =	6
R_s' =	12.5
R_s =	0.4 ohms

The maximum line power sustainable by the duplexer is calculated

from Equation (19) to be 4.5 kilowatts per diode. Since a peak power of 15 kilowatts per limiter chain is required, four diodes are necessary.

The impedance level at which switching is performed may now be calculated using Equation (14).

$$n_3^2 \approx \frac{(I.L._m)\ R_s'\ Q^2}{Z_o} \qquad (14)$$

Where R_s' is the effective transmission state resistance of four line shunting diodes and, thus, is equal to one quarter the value of a single diode.

$$R_s' = \frac{12.5 \text{ ohms}}{4}$$

Equation (14) may be solved and found to yield a value of n_3^2 equal to 0.225. This is the ratio of the effective switching impedance to the characteristic impedance of the system of which the duplexer is used. For a coaxial circuit Z_o is typically 50 ohms and thus the impedance level at which switching should be performed is approximately 11 ohms.

The isolation which would be obtained by four diodes at this switching level whose isolating state resistance is 0.4 ohms would be only 40 db, and 55 db is required to assure that the receiver power level does not exceed 100 milliwatts peak. This can be achieved by placing an additional diode in the transmission line spaced a quarter wavelength from the four diodes previously discussed. This circuit is diagrammed

in Figure 9. The value of the conductance, Y_2 need be only 10 times the characteristic switching admittance, and therefore, a single diode having an isolation state resistance of 1 ohm would be adequate. The additional insertion loss obtained at low level resulting from this diode should be quite small and will be neglected in this discussion.

The bandwidth of this receiver protector design will be a function not only of the transmission state and isolation state Q values of the switching elements but also of the transformers which would consist typically of quarter wavelengths of transmission line and the quarter wavelength spacing of the two diode switching stages. Analysis of the bandwidth for the two states has not been carried out. However, it is believed that serious bandwidth limitations will not be imposed by this circuitry on the basis of experience gained in previously built microwave transformer circuits. Efforts in the coming quarter will be to make and evaluate these receiver protector circuit design criteria.

4. Conclusions

An evaluation of thin base PIN diodes was performed at 420 mc. The minimum isolation state resistance was found equal to 0.32 ohms and the transmission state resistance was 12.5 ohms in series with a 5 pf capacitance, yielding a reverse bias Q of 6. The power which may be dissipated in the diode during a 60 microsecond pulse was calculated assuming a die temperature rise of 200° Centigrade and no cooling within the pulse to be 160 watts. This value together with the diode impedance parameters and desired transmission state insertion loss of 0.5 db was shown to limit the maximum incident RF power in an ideally designed

duplexer circuit containing the diode to 4.5 kilowatts. Four such diodes, then are necessary to control the 15 kilowatt peak power, which is the design objective for a single limiter chain.

The impedance level at which switching should be performed was calculated to be 11 ohms. An isolation of 40 db should be obtained by the diodes with forward resistances of 0.4 ohms, and an additional diode having 1 ohm or less resistance and placed a quarter wavelength behind the previous four in the 11 ohm line is required to achieve the 55 db minimum isolation desired to prevent the receiver level power from exceeding 100 milliwatts peak.

Efforts will be directed in this coming quarter to fabricate and analyze this limiter circuit.

PART II

PROGRAM FOR THE NEXT INTERVAL

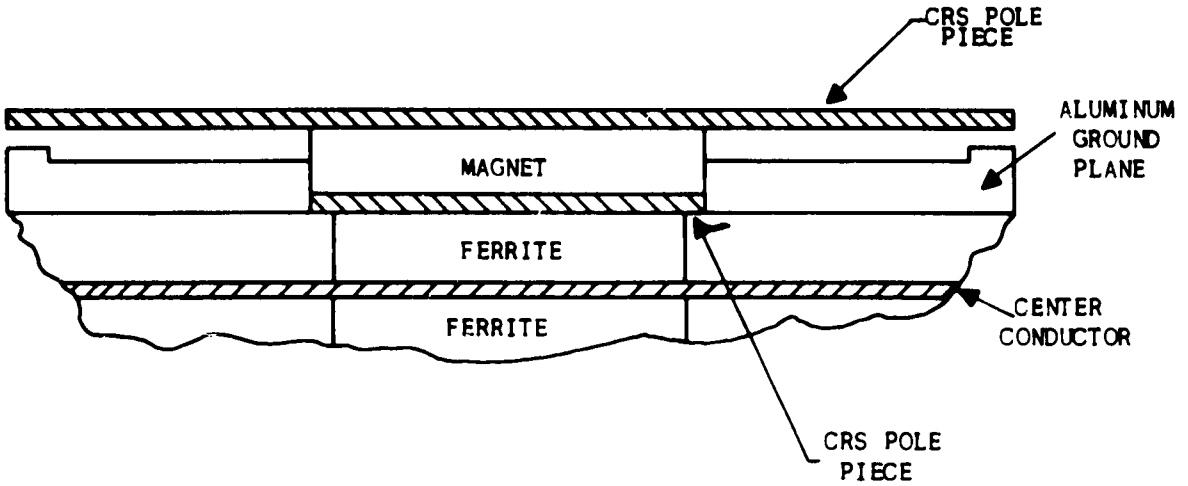
1. Completion of the 420 Mc circulator with the required bandwidth, isolation, insertion loss and VSWR parameters.
2. Parts purchasing for the 210 Mc circulator.
3. Completion of the test facilities for 60 μs pulse width testing.
4. Evaluation of the PIN diode limiter at increased pulse width and duty cycle.
5. Fabrication and evaluation of the switching circuit designed to achieve the required 55 db receiver isolation.

PART III

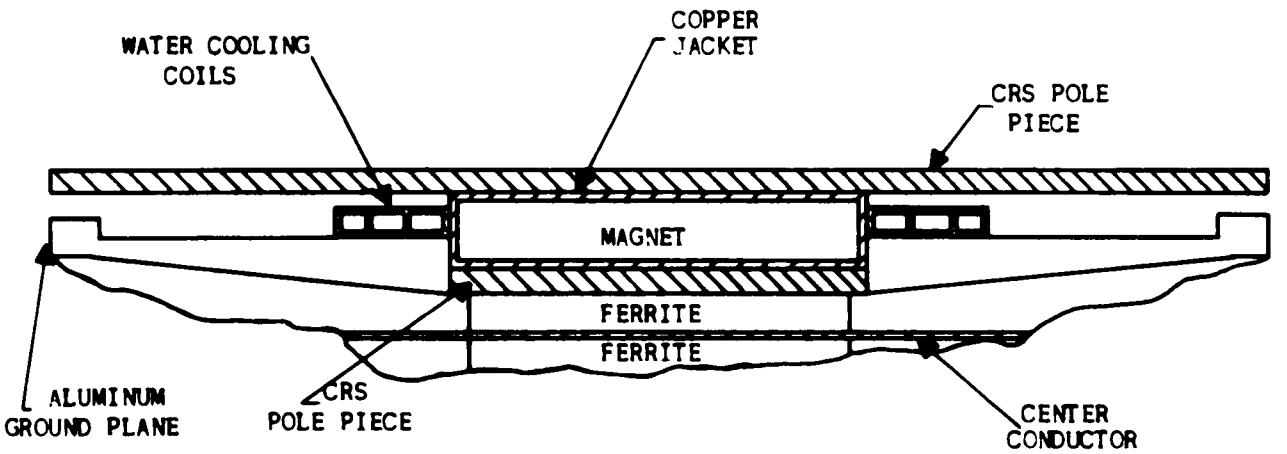
LIST OF ILLUSTRATIONS

FIGURE 1

CIRCULATOR DESIGN APPROACHES



a) FLAT GROUND PLANE - AIR COOLED UNIT



b) TAPERED GROUND PLANE - WATER COOLED UNIT

FIGURE 2

Low Power ISOLATION AND INSERTION LOSS
VS.
FREQUENCY

GARNET G1002 .400 THICK

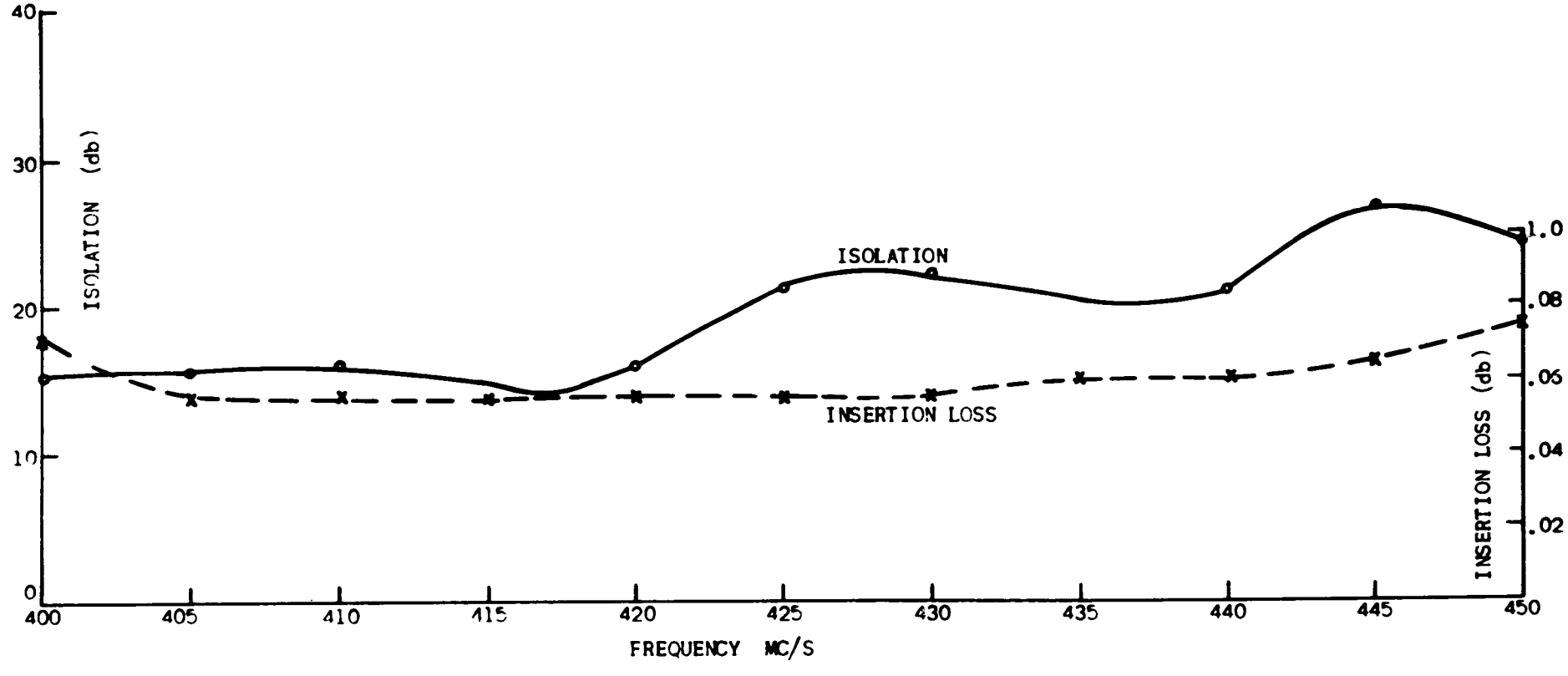


FIGURE 3

High Power ISOLATION AND INSERTION LOSS
VS.
TEMPERATURE

INPUT 500 WATTS
TOTAL TEST TIME 51 MIN.
420 MC/S UNIT GARNET G1002 .400 THICK

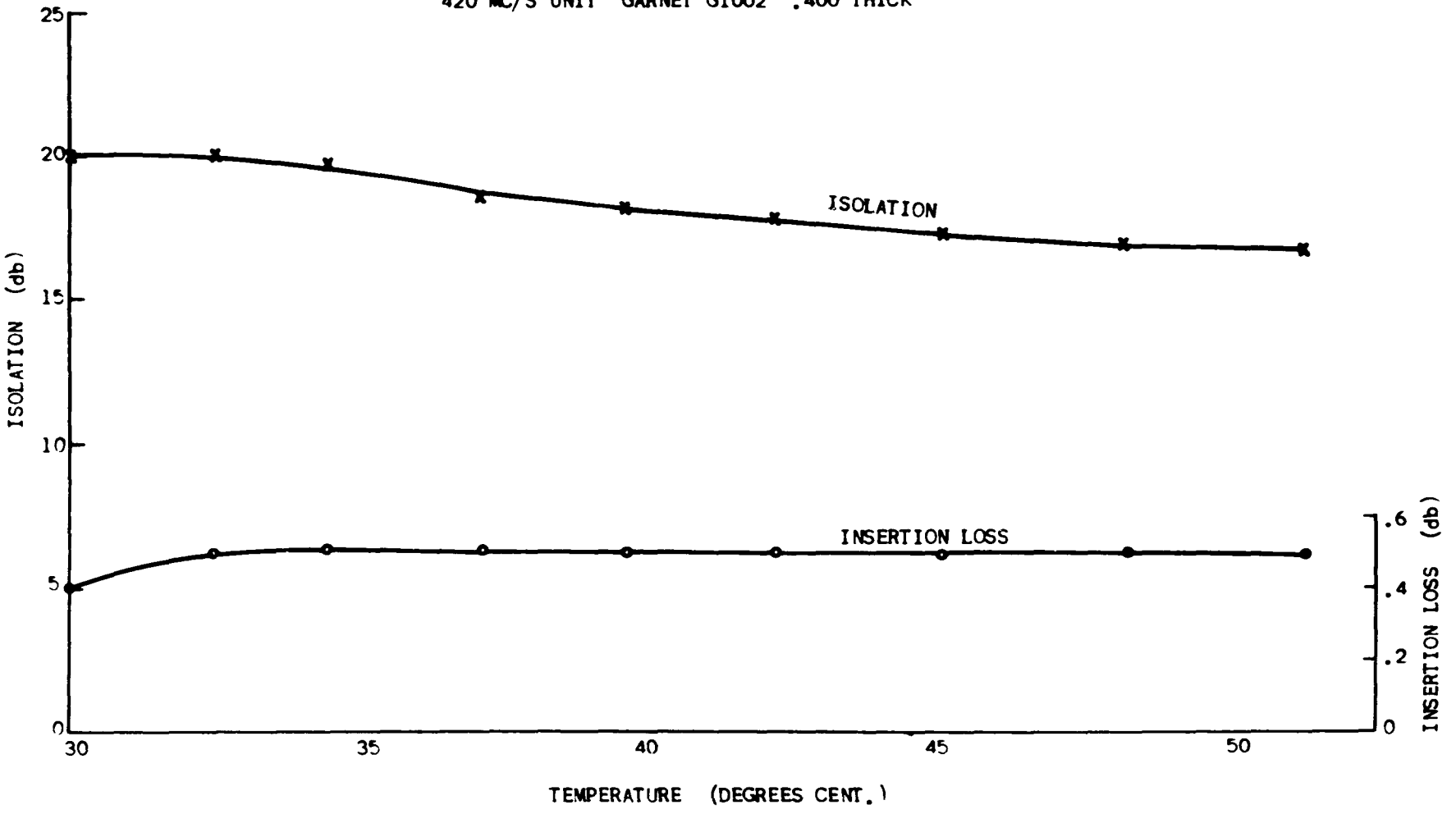
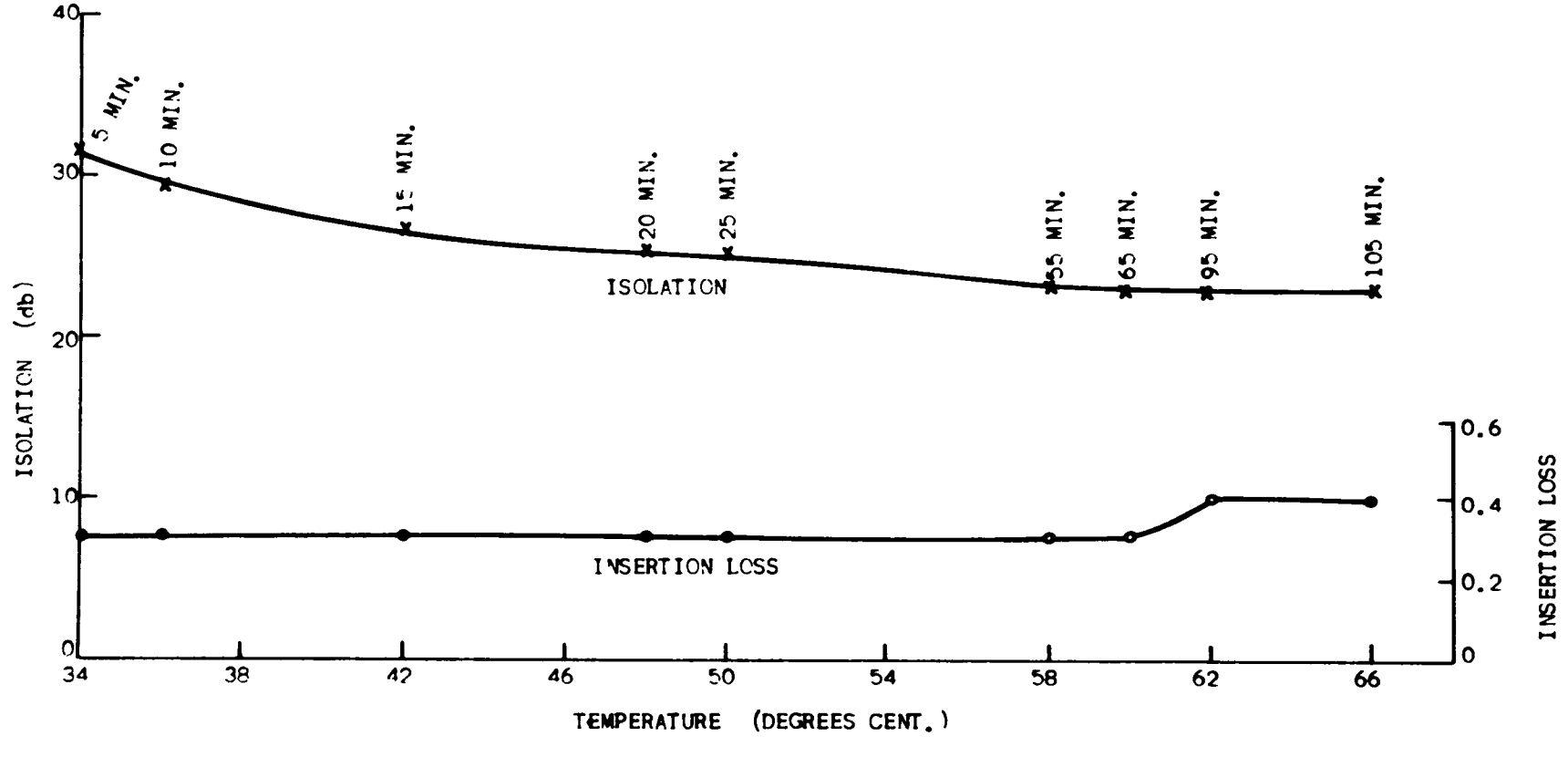
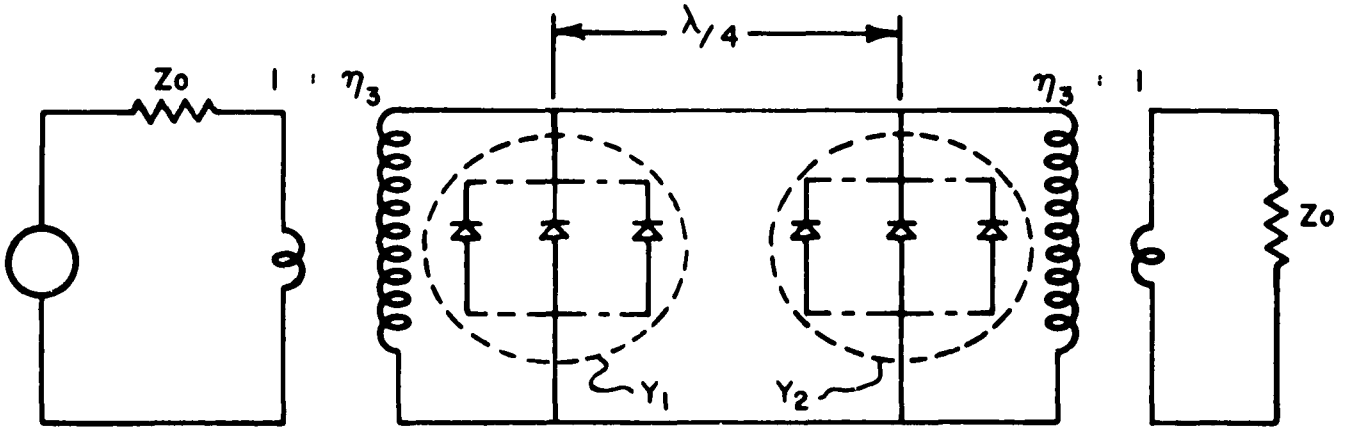


FIGURE 4

High Power ISOLATION AND INSERTION LOSS
VS.
TEMPERATURE

INPUT POWER 1500 WATTS CW
TOTAL TEST TIME 1 HR. 45 MIN.
400 MC/S UNIT GARNET G1002 .200 THICK





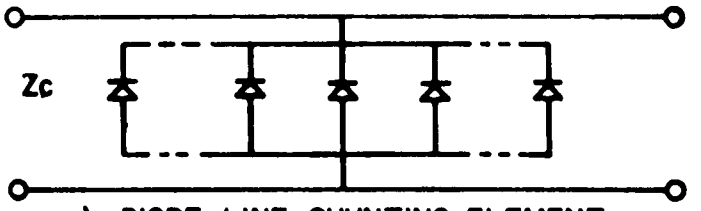
DEFINE SWITCHING IMPEDANCE = Zo

$$Zs = \eta_3^2 \times Zo$$

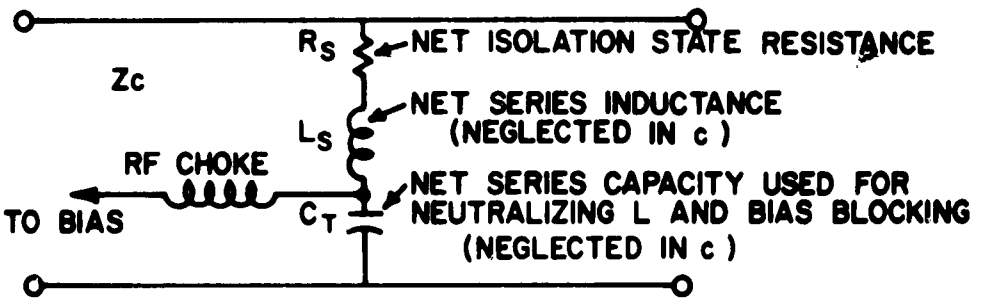
$$\text{ISOLATION} = \frac{Y_1^2 \times Y_2^2 \times Zo^4 \times n_3^2}{4}$$

TWO STAGE LIMITER UTILIZING IMPEDANCE TRANSFORMERS

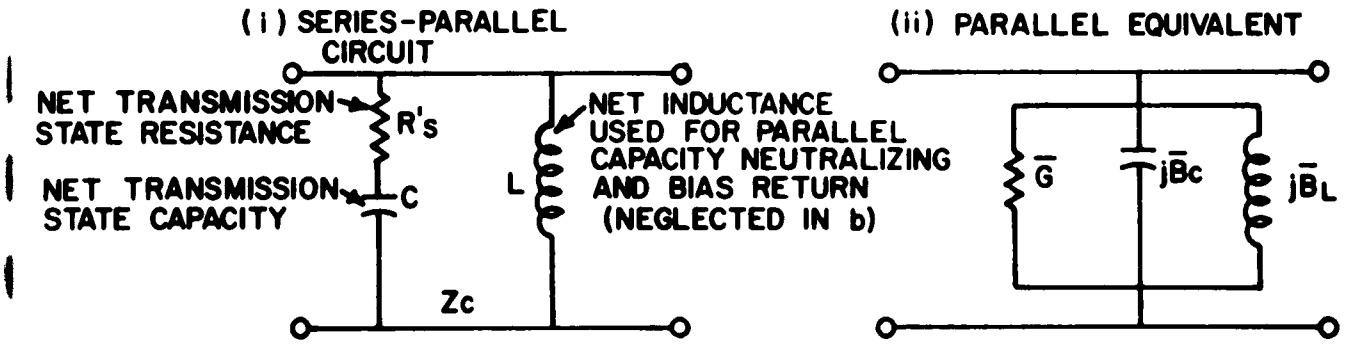
FIGURE 9



a) DIODE, LINE SHUNTING ELEMENT



b) ASSUMED ISOLATION STATE EQUIVALENT CIRCUIT



DEFINE $\bar{R}'_S = R'_S/Z_c$

$$Q = \frac{1}{\omega C R'_S}$$

WHERE $\bar{G} = \dfrac{1}{\bar{R}'_S(1+Q^2)}$

$$j\bar{B}_C = \frac{+jQ}{\bar{R}'_S(1+Q^2)}$$

$$j\bar{B}_L = \frac{j}{\omega L}$$

c) ASSUMED TRANSMISSION STATE EQUIVALENT CIRCUIT

FIGURE 10

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Contract No. NObsr 89105

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